REMARKS

Favorable reconsideration of this application is respectfully requested.

With respect to the objection to the Title, applicants believe the Title is clearly directed to the claim features, but if the Examiner has a proposed new Title applicants will consider such.

Addressing now the claim objections, claims 1-16 are amended to no longer refer to "a register body" but now instead only and consistently refer to a "register part". Those amendments are believed to clarify the claim language and address the objections thereto. Applicants also submit the claims are proper and clearly describe the concept of the present invention, which applicants do not agree is a "simple concept", as discussed in further detail below.

Claims 1-16 are pending in this application. Claims 1-16 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent Application Publication 2003/0217249 to Postiff et al. (herein "Postiff") in view of U.S. patent 6,189,087 to Witt et al. (herein "Witt"). That rejection is traversed by the present response as discussed next.

The outstanding rejection relies on Postiff to disclose each claimed feature except for the "instruction code being obtained by pre-decoding the instruction from said instruction fetch part", and the outstanding rejection relies on Witt to disclose that feature at column 7, line 64 to column 8, line 16.[1]

In reply to that basis for the rejection applicants respectfully submit the claims as written distinguish over Postiff in view of Witt.

The claims are directed to a processor that includes a register renaming function for sequentially rewriting contents of a register alias table using a reorder buffer and a physical register free list, the reorder buffer holding a correspondence of a local register number to its

[1] Office Action of September 15, 2006, page 4, last full paragraph.

physical register number, which are included in the decoded instruction code, in a register alias table and storing an assignable number of the physical register number in the physical register free list to store a correspondence of an instruction number, an architecture register number, and an old physical register number.

First, applicants submit Witt does not cure the recognized deficiencies in Postiff as Witt does not disclose or suggest the "instruction code being obtained by pre-decoding the instruction from said instruction fetch part".

More specifically, Witt merely describes that:

> ... x86 instructions... are parsed and pre-decoded in an instruction cache ("ICACHE") 104, the pre-decoded x86 instructions are copied to a byte queue ("BYTEQ") 106, and the pre-decoded x86 instructions are mapped in an instruction decoder ("IDECODE") 108 to respective sequences of instructions for RISC-like operations ("ROPs").[2]

From the above-disclosure it is clear that Witt merely discloses that the fetched instruction code is parsed or divided into x86 instructions, which are mapped to respective sequences of instructions for ROPs.

In contrast to that disclosure in Witt, and with reference to Figures 1 and 2 in the present specification as non-limiting examples, in the present invention a register transfer and issuing part (for example element 9 in Figure 1, element 120 in Figure 2) issues a register transferring instruction for transferring inner data between the caching register (for example element 3 in Figure 1, element 300 in Figure 2) and the register part (for example element 4 in Figure 1, element 400 in Figure 2) when the instruction insertion determining part determines that the inner transfer function is to be inserted.

Witt merely discloses generating a plurality of instructions by parsing or dividing one fetched instruction. The claims are not directed to such an operation as in Witt but instead

[2] Witt at column 4, lines 11-18.

the claims are directed to issuing a register transfer function. In the claimed subject matter the fetched and instruction group does not include information with respect to "the register transfer function", and the issuing part issues "the register transfer instruction" on the basis of the register numbers and the fetched instructions.

In such ways applicants respectfully submit Witt does not cure the recognized deficiencies in Postiff.

Moreover, applicants submit Postiff does not even disclose all the claimed features relied upon in the basis for the outstanding rejection. That is, Postiff is further deficient than as recognized in the Office Action.

One basis for the outstanding rejection cites paragraph [0035] of Postiff to disclose a "register transfer instruction issuing part configured to issue a register transfer instruction for transferring inner data between said caching register and said register body when the instruction insertion determining part determines that the inner transfer instruction is to be inserted". Applicants traverse that basis for the outstanding rejection. Specifically, Postiff in paragraph [0035] merely states:

> Readiness is determined in when a producer instruction 108 (see FIG. 4) completes and broadcasts its VRN 105 to the reservation stations. Each station compares its unready source VRN with VRN 105 broadcasted. If there is a match, the source VRN is marked ready. When all the instruction's operands become ready, the instruction is scheduled (selected) for execution. The low 6 bits of the instructions operand source VRN are used to directly index into the 64-entry PRF 10 (branch 52 of FIG. 3).

Applicants submit that disclosure in Postiff does not correspond to the "register transfer instruction issuing part" in the claims. Specifically that disclosure in Postiff does not indicate any transfer of inner data between a caching register (for example element 3 in Figure 1, element 300 in Figure 2) and a register part (for example element 4 in Figure 1,

element 400 in Figure 2) based on determining that an inner transfer instruction is to be inserted.

Moreover, applicants submit that in Postiff the producer operand supplied from the producer instruction 108 to the physical register file 10 would correspond to RISC-like operations (ROPs) such as in Witt, as Postiff states in the above-noted paragraph [0035] that "the low 6 bits of the instructions operand source VRN are used to directly index into the 64-entry PRF 10".

In view of the foregoing comments applicants respectfully submit the claims as written positively recite features neither taught nor suggested by Postiff in view of Witt. Applicants submit neither of those references disclose or suggest that a register transfer instruction for transferring inner data between a caching register (for example element 3 in Figure 2, element 300 in Figure 2 in the present specification) and the register part (for example element 4 in Figure 1, element 400 in Figure 2 in the present specification) when the instruction insertion determining part determines that the inner transfer instruction is to be inserted. Thereby, applicants respectfully submit the claims as written distinguish over Postiff in view of Witt.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

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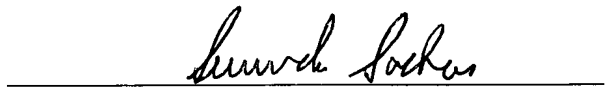

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